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# 1 [Performance debugging shared memory parallel programs using run-time dependence analysis](#)

Ramakrishnan Rajamony, Alan L. Cox

 June 1997 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1997 ACM SIGMETRICS international conference on Measurement and modeling of computer systems**, Volume 25 Issue 1

Full text available: pdf(2.37 MB)

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We describe a new approach to performance debugging that focuses on automatically identifying computation transformations to reduce synchronization and communication. By grouping writes together into *equivalence classes*, we are able to tractably collect information from long-running programs. Our performance debugger analyzes this information and suggests computation transformations in terms of the source code. We present the transformations suggested by the debugger on a suite of four ap ...

# 2 [Replay for concurrent non-deterministic shared-memory applications](#)

Mark Russinovich, Bryce Cogswell

 May 1996 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 1996 conference on Programming language design and implementation**, Volume 31 Issue 5

Full text available: pdf(968.81 KB)

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Replay of shared-memory program execution is desirable in many domains including cyclic debugging, fault tolerance and performance monitoring. Past approaches to repeatable execution have focused on the problem of re-executing the shared-memory access patterns in parallel programs. With the proliferation of operating system supported threads and shared memory for uniprocessor programs, there is a clear need for efficient replay of concurrent applications. The solutions for parallel systems can b ...

**Keywords:** instruction counter, non-determinism, repeatable execution, shared memory

# 3 [Parasight: a high-level debugger/profiler architecture for shared-memory multiprocessor](#)

Z. Aral, Ilya Gertner

 June 1988 **Proceedings of the 2nd international conference on Supercomputing**

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### 1 [Parasight: a high-level debugger/profiler architecture for shared-memory multiprocessor](#)

Z. Aral, Ilya Gertner

 June 1988 **Proceedings of the 2nd international conference on Supercomputing**

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Existing debuggers and profilers are inadequate for debugging and profiling parallel programs. They are awkward in their handling of multiple threads of control and highly intrusive in their monitoring of program behavior. Parasight<sup>TM</sup> is an architecture that is geared towards non-intrusive high-level debugging and profiling. Parasight controls and observes the execution of parallel programs in terms of the set of abstractions that are being employed by the programmer. D ...

### 2 [Efficient debugging primitives for multiprocessors](#)

Z. Aral, I. Gerther, G. Schaffer

 April 1989 **ACM SIGARCH Computer Architecture News , Proceedings of the third international conference on Architectural support for programming languages and operating systems**, Volume 17 Issue 2

Full text available: pdf(792.54 KB)

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Existing kernel-level debugging primitives are inappropriate for instrumenting complex sequential or parallel programs. These functions incur a heavy overhead in their use of system calls and process switches. Context switches are used to alternately invoke the debugger and the target programs. System calls are used to communicate data between the target and debugger. None of this is necessary in shared-memory multiprocessors. Multiple processors concurrently run both the debugge ...

### 3 [Hardware support for program debuggers in a paged virtual memory](#)

David Abramson, John Rosenberg

 June 1983 **ACM SIGARCH Computer Architecture News**, Volume 11 Issue 2

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### 4 [Tera hardware-software cooperation](#)

Gail Alverson, Preston Briggs, Susan Coatney, Simon Kahan, Richard Korry

 November 1997 **Proceedings of the 1997 ACM/IEEE conference on Supercomputing**


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Rafael Alonso, Daniel Barbara, Hector Garcia-Molina

 September 1990 **ACM Transactions on Database Systems (TODS)**, Volume 15 Issue 3

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Currently, a variety of information retrieval systems are available to potential users.... While in many cases these systems are accessed from personal computers, typically no advantage is taken of the computing resources of those machines (such as local processing and storage). In this paper we explore the possibility of using the user's local storage capabilities to cache data at the user's site. This would improve the response time of user queries albeit at the cost of incurring t ...

**Keywords:** cache coherency, data sharing, information retrieval systems

### 2 [A portable interface for on-the-fly instruction space modification](#)

David Keppel

 April 1991 **Proceedings of the fourth international conference on Architectural support for programming languages and operating systems**, Volume 19 , 25 , 26 Issue 2 , Special Issue , 4

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### 3 [The VMP multiprocessor: initial experience, refinements, and performance evaluation](#)

D. R. Cheriton, A. Gupta, P. D. Boyle, H. A. Goosen

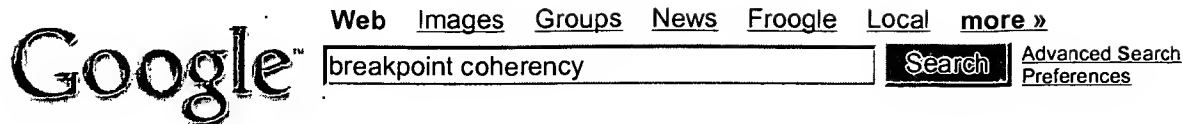
 May 1988 **ACM SIGARCH Computer Architecture News , Proceedings of the 15th Annual International Symposium on Computer architecture**, Volume 16 Issue 2

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VMP is an experimental multiprocessor being developed at Stanford University, suitable for high-performance workstations and server machines. Its primary novelty lies in the use of software management of the per-processor caches and the design decisions in the cache and bus that make this approach feasible. The design and some uniprocessor trace-driven simulations indicating its performance have been reported previously. In this paper, we present our initial experience with the V ...

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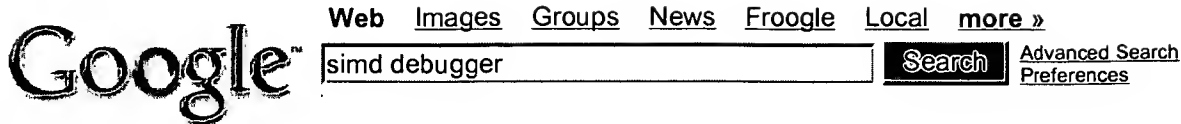
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Z. Aral, Ilya Gertner

June 1988 **Proceedings of the 2nd international conference on Supercomputing**Full text available: [pdf\(764.60 KB\)](#)Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Existing debuggers and profilers are inadequate for debugging and profiling parallel programs. They are awkward in their handling of multiple threads of control and highly intrusive in their monitoring of program behavior. Parasight<sup>TM</sup> is an architecture that is geared towards non-intrusive high-level debugging and profiling. Parasight controls and observes the execution of parallel programs in terms of the set of abstractions that are being employed by the programmer. D ...

# 2 [A bibliography of parallel debuggers, 1990 edition](#)

Cherri M. Pancake, Sue Utter

January 1991 **ACM SIGPLAN Notices**, Volume 26 Issue 1Full text available: [pdf\(1.55 MB\)](#)Additional Information: [full citation](#), [citations](#), [index terms](#)

# 3 [A bibliography of parallel debuggers, 1993 edition](#)

Cherri M. Pancake, Robert H. B. Netzer

December 1993 **ACM SIGPLAN Notices , Proceedings of the 1993 ACM/ONR workshop on Parallel and distributed debugging**, Volume 28 Issue 12Full text available: [pdf\(1.17 MB\)](#)Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

# 4 [A "flight data recorder" for enabling full-system multiprocessor deterministic replay](#)

Min Xu, Rastislav Bodik, Mark D. Hill

May 2003 **ACM SIGARCH Computer Architecture News , Proceedings of the 30th annual international symposium on Computer architecture**, Volume 31 Issue 2Full text available: [pdf\(311.95 KB\)](#)Additional Information: [full citation](#), [abstract](#), [references](#)

Debuggers have been proven indispensable in improving software reliability. Unfortunately, on most real-life software, debuggers fail to deliver their most essential feature --- a faithful replay of the execution. The reason is non-determinism caused by multithreading and non-repeatable inputs. A common solution to faithful replay has been to record the non-deterministic execution. Existing recorders, however, either work only for data-race-free